REMARKS

Claims 1-24 are pending of which independent claims 1, 15, 18, 22, 23 have been amended and the claims 2, 23 has been cancelled without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to claims. For at least the foregoing reason, Applicants respectfully submit that claims 1, 3-22 and 24 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of amendments to claims 1, 15, 18

From paragraph [0044], there discloses "In the embodiment described in Fig. 3, the basic conception of the time delay synchronous control circuit 170 is to make sure the buck switches Q_1 and Q_2 of the post buck converters 130 and 140 draws pulse currents from the output capacitor Cf_1 only during the time when the diode D_1 or D_2 has conduction current." Thus, during the time when the front-end converter has the pulse output current to the first output capacitor, the charging current of the first output capacitor is the difference between the pulse output current from the front-end converter 110 (shown in Fig.3) and the pulse current drawn by the first buck converter and the second buck converter. Hence, a limitation "a charging current of

the first output capacitor is a difference between the pulse current output from the front-end converter and the pulse current drawn by the first buck converter and the second buck converter" is added into claim 1 without introducing any new matter.

Discussion of claim objections

Claims 23 and 24 are objected because there is insufficient antecedent basis for recitation "The synchronous control scheme of claim 22" as claimed in claims 23, 24.

In response thereto, claim 23 is canceled, and subject matter of claim 24 is amended from "The synchronous control scheme of claim 22" to "The power supply of claim 22."

Discussion of rejection to claims under 35 U.S.C. §103(a)

Claims 1, 15, 18 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Bourdillon (U.S. Patent No.6, 552, 917).

In response thereto, applicant respectfully traverses the rejection based on the following arguments. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference themselves or in the

knowledge generally available to one of ordinary skill in the art, to modify the references or to combine references teachings. Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.**

In re claim 1, claim 1 is amended and partly recited as follows.

1. A power supply with multiple outputs, comprising:

the first buck converter and the second buck converter draw pulse current from the first output capacitor, **and the charging current of the first output capacitor is the difference between the pulse current output from the front-end converter and the pulse current drawn by the first buck converter and the second buck converter** during the time when the front-end converter has the pulse output current to the first output capacitor, **and the front-end converter is an LLC-SRC.**

From Fig.3, in Bourdillon, no claimed first output capacitor is disclosed. Hence, Bourdillon fails to disclose claimed "a charging current of the first output capacitor." Also, Bourdillon fails to disclose "a charging current of the first output capacitor is a difference between the pulse current output from the front-end converter and the pulse current drawn by the first buck converter and the second buck converter" as claimed in claim 1. More, AAPA

(applicant's admitted prior art) fails to disclose "a charging current of the first output capacitor (i.e. Cf) is a difference between the pulse current output from the front-end converter and the pulse current drawn by the first buck converter and the second buck converter," as claimed in claim 1.

Additionally, claim 1 is amended to merge claim 2 so as to incorporate a limitation "the front-end converter is an LLC-SRC." Since output current from the front-end converter is quasi-sine pulse shape (see timing diagrams of i_{D1}, i_{D2}, in Fig.4 in the specification), the pulse shape cause serious ripple current of the first output capacitor. Thus, the claimed time delay synchronous control circuit is needed to be implemented for the front-end converter to reduce the ripple current of the first output capacitor. In contrast, conventional pulse width modulation (PWM) circuit outputs pulses with continual saw-tooth shape, which inherently cause the first output capacitor to have small ripple current. Hence, the claimed time delay synchronous control circuit is not needed to be implemented for the conventional PWM circuit. In other words the claimed invention will reduce the great ripple current in LLC-SRC and none of the prior art has disclose it. Even if AAPA could be combined with Bourdillon, the combination still fails to disclose aforementioned underlined features. That is, amended claim 1 is not rendered obvious by AAPA and Bourdillon, and accordingly patentable.

In re claims 15, 18 and 22, by using the same arguments as applied to amended claim 1, the amended claims 15, 18 and 22 are also not rendered obvious by AAPA and Bourdillon, and accordingly patentable.

Claims 2-14, 16-17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Bourdillon (U.S. Patent No.6,552,917) in further view of Huang (U.S. Patent No.6,344,979)

In response thereto, applicant respectfully traverses the rejection based on the following arguments. Since claims 3-14, 16-17 and 19-21 are dependent claims, they should be patentable for the reason that they contain all limitations of their patentable base independent claims 1, 15 and 18.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 3-22 and 24 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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